

REMARKS

Claim 1 calls for implementing read accesses to the same portion of a memory line in the same cycle.

The Examiner cites portions of the patent to Kawasaki which discuss things like simultaneous access. Examples of what Kawasaki calls simultaneous access include a load-load command, load-store command, store-load command, and store-store command. See column 1, lines 58-61.

The problem is that what Kawasaki talks about as a “simultaneous access” is clearly not a simultaneous access and Kawasaki engineers his system to ensure that there is no simultaneous access, believing that such a result apparently would be undesirable. He goes on to explain that:

Namely, there occurs a simultaneous access at the same address, therefore, a data guaranteed based on the order of the load-store command becomes necessary. The data guarantee means that when the store command is executed after the load command, it shall be guaranteed that the data is loaded before the data is stored for a particular cache memory address.

See column 1, lines 61-67.

Thus, the so-called load-store simultaneous command is executed in series, the first command being executed before the second command. Therefore, there are not read accesses to the same portion of the memory line in the same cycle.

In other words, even though Kawasaki says these are simultaneous accesses, he handles these alleged simultaneous accesses in a way that ensures that they occur serially. He does not access the same portion of the memory line in the same cycle but, instead, does so in two successive cycles. In effect, it seems that his invention could be that, instead of accessing the same portion of the memory line in a same cycle, when he sees a situation that would apparently call for such a result, the commands are transformed so that they incur one after the other.

Therefore, reconsideration of the rejection of claim 1 is respectfully requested. On the same basis, reconsideration of the other claims would be appropriate.

Respectfully submitted,



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